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	LIQUID CRYSTAL DISPLAY GROUP SHARP CORPORATION	APPLICABLE GROUP Liquid Crystal Display Group
	SPECIFICATION	

DEVICE SPECIFICATION FOR

MODEL No. LQ5RA43

☐ CUSTOMER'S APPROVAL

DATE

BY

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CONTENTS

(1)Introduction'

Sharp Color TFT-LCD module is the active matrix LCD (Liquid Crystal Display) produced by making the ❑ ost of Sharp's expertise in liquid-crystal and semiconductor technologies. The active device is amorphous silicon TFT (Thin Film Transistor). The module accepts full color video signal conforming to the NTSC(M) and PAL(B·G) system standards.
When additionally provided with the backlight system and a circuit for producing standard analog R·G·B video signals from composite video signal or micro-computers, it is applicable to pocket TVs and various display monitors. It is superior of reliability and just fit into 2 DIN size.

(2)Features

.Dual mode type. [NTSC(M) and PAL(B·G) standards]

● MBK-PAL, or blaBiKi("thinning" in Japanese)-PAL which enables the 234-scanning lines panel to display a picture with virtually 273-scanning lines.

● TFT-active matrix -LCD drive system with high-contrast.

● 74,880 pixels (RGB Stripe configuration and full color) in 5" diagonal.

• Slim, lightweight and compact

①Active area/Outline area = 70% ②Thickness :23. 7mm ③Mass :165 g

• Built-in video interface circuit and control circuit responsive to two sets of standard R·G·B analog video signals.

• Low reflection black matrix and an anti-reflection front polarizer are used.

● Optimal viewing angle : 6 o'clock direction. (HRV, VRV=' Hi')

• It is possible to make a picture reverse.

• An external clock mode is available.

• It is possible to use both the same and the independent time sampling.

(3)Construction and Outline

"Illustration of TFT-LCD panel : See Fig. 1

● Construction of TFT-LCD module : See Fig. 2

"Outline dimensions of TFT-LCD module: See Fig. 3

•The module consists of a TFT-LCD panel, driver ICS, control PWB mounted with electronic circuits, diffuser, frame, front and rear shielding cases.
(Backlight excluded from the module.)

(4)Module geometry(Mechanical specification)

Tabel 1

Parameter	Specification	Unit	Remarks
Display format	74,880 960(H) × 234(V)	Pixels dots	
Active area	102. 7(H)x 74.9 (V)	mm	
Screen size (Diagonal)	13 [5" 1	cm	
Dot pitch	0.107(H)X0.320 (V)	mm	
Dot configuration	R·G·B Stripe configuration		
Outline dimension	122. 6(W) X89. 6(H) X23.7(D)	mm	[Note 4-1]
Mass	165 ± 10	g	

[Note 4-l]This measurement is typical, and in detail, see figure of outline .

(5) Input/output terminals and their descriptions

-5-1)TFT-LCD panel driving section (Hi means digital input high voltage, Lo means GND.)

Table 2

Pin No.	Symbol	i/o	Description	Remarks
1	$\overline{HSY}$	i , o	Input/output horizontal sync. signal (low active)	[Note 5-1]
2	$\overline{VSY}$	i , o	Input/output vertical sync. signal (low active)	[Note 5-21
3	TST	o	This should be electrically opened during operating.	
4	NTP	i	Terminal for display mode change of NTSC and PAL	[Note 5-31
5	HRV	i	Turning the direction of horizontal scanning	[Note 5-41
6	VRV	i	Turning the direction of vertical scanning	[Note 5-51
7	VSW	i	Selection signal of two sets of video signals	[Note 5-61
8	SAM	i	Terminal for sampling mode change	[Note 5-71
9	V_{CDC}	i	DC bias voltage adjusting terminal of common electrode driving signal	[Note 5-81
10	VSH	i	Positive power supply voltage	
11	$\overline{VBS}$	i	Composite video signal for sync. separator	[Note 5-91
12	BRT	i	Brightness adjusting terminal	[Note 5-101
13	VR1	i	Color video signal (Red) 1	Positive (On when VSW=Hi.)
14	VG1	i	Color video signal (Green) 1	Ditto
15	VB1	i	Color video sisal (Blue) 1	Ditto
16	VSL	i	Negative power supply voltage	
17	VR2	i	Color video signal (Red) 2	Positive (On when VSW=Lo.)
18	VG2	i	Color video signal (Green) 2	Ditto
19	VB2	i	Color video signal (Blue) 2	Ditto
20	GND	i	Ground	
21	CLKC	i	Change the input/output direction of CLK. HSY and VSY	[Note 5-11]
22	CLK	i , o	Input/output clock signal	[Note 5-12]

[Note 5-1] If CLKC=' Hi', this terminal outputs horizontal sync. signal in phase with $\overline{VBS}$.
If CLKC=' LO', this terminal will be external horizontal sync. input terminal.

[Note 5-21 If CLKC=' Hi', this terminal outputs vertical sync. signal in phase with $\overline{VBS}$.
If CLKC='Lo', this terminal will be external vertical sync. input terminal.

[Note 5-31 This terminal is to switch display mode, and it is NTSC mode when NTP is 'High' and is PAL mode when NTP is 'Low'.

[Note 5-41 When this terminal is 'High', it will be normal and when it is 'Low', it will display reversely on horizontal direction.

[Note 5-51 When this terminal is 'High', it will be normal and when it is 'Low', it will display reversely on vertical direction.

[Note 5-61 This terminal is to switch input for groups of R,G,B color video signals, and Input 1 (No. 13 to 15) is selected when VSW is 'High' and Input 2 (No. 17 to 19) is selected when VSW is 'Low'.

[Note 5-7] This terminal is to switch sampling mode. It is the different data-sampling timing at RGB dots when SAM is 'High' and it is the same data-sampling timing at RGB dots when SAM is 'Low'.

[Note 5-81 This terminal is applicable to the DC bias voltage adjusting terminal of common electrode driving signal. If power supply voltage is typical, it is not necessary to re-adjust it, so use it in the open condition.
However, in the case that power supply voltage is changed, or power supply voltage is reduced, please adjust it externally to get the best contrast with a resistor You add to this terminal, or semifixed resistor, VCDC, in module. A recommended circuit is shown in Fig. 5.

[Note 5-9] The sync. signal which will be input, is negative polarity, and is applicable to standard composite sync. signal, negative one, in the same pulse level.

[Note 5-10] DC voltage supplied charged to this terminal, make the brightness of screen adjustable, that is, the black level of video signal adjustable.
Adjusting it in the time of delivery to get the best display in the condition of open terminal, You will be able to re-adjust it externally with a resistor you add to this terminal, or a semifixed resistor, BRT, in module. A recommended circuit is shown in Fig. 5.

[Note 5-11] CLKC='Hi' :CLK, $\overline{HSY}$, $\overline{VSY}$ terminals are output mode.
CLKC='LO' :CLK, $\overline{HSY}$, $\overline{VSY}$ terminals are input mode.

[Note 5-12] If CLKC=' Hi', this terminal outputs 'Lo' voltage level.
If CLKC=' LO', this terminal will be external clock input terminal.

Caution:The shielding case is separated from GND terminal and electrically open.

5-2) Functional reaching and Input/Output mode

Table 3

Terminal	CLKC="Hi"		CLKC="Lo"	
	SAM="Hi"	SAM="Lo"	SAM="Hi"	SAM="Lo"
$\overline{HSY}$	output	output	Input	Input
$\overline{VSY}$	output	output	Input	Input
CLK	Output "Lo voltage"	Output "Lo voltage"	Input "Dot clock"	Input "Pixel clock"

(6) Absolute maximum ratings

Table 4 GND=OV. Ta=25°C

Parameter	Symbol	MIN	MAX	Unit	Remarks
Positive power supply voltage	V_{SH}	-0.3	-9.0	V	
Negative power supply voltage	V_{SL}	-6.0	+0.3	V	
Analog input signals	Vi	—	2.0	V p-p	[Note 6-1]
Digital input/output signals	VI	-0.3	-5.4	V	[Note 6-2]
'DC bias voltage of common electrode driving signal	V_{CDC}	V_{SL}	V_{SH}	V	
Brightness adjusting terminal	V_{BRT}	0	+5.1	V	
Storage temperature	Tstg	-30	85	℃	[Note 6-3]
Operating temperature	Top	-30	85	℃	[Ditto]

[Note 6-1] $\overline{VBS}$, VR1, VG1, VB1, VR2, VG2, VB2 terminals(Video signal)

[Note 6-2] NTP, HRV, VRV, SAM, VSW, $\overline{HSY}$, $\overline{VSY}$, CLKC, CLK terminals

[Note 6-3] Maximum wet-bulb temperature less than 58℃. Do not dew condensation. Dew condensation may cases electrical leaks and the specification described here may not be satisfied. In the condition that backlight is not on, these temperatures are measured. Panel facial temperature should not exceed 85℃ due to the heat generation of lamp.

(7)Electrical characteristics

7-1) Recommended 'operating condition

able 5 GND=OV. T a =25℃

Parameter		Symbol	MIN	TYP	MAX	Unit	Remarks
Positive power supply voltage		V_{SH}	+7.8	+8.0	+8.2	V	[Note 7-1]
Negative power supply voltage		V_{SL}	−5.2	−5.0	-4.8	V	
Analog input voltage	Amplitude	VBS	0.7	1.0	2.0	Vp-p	Input resister
		Vi	-	0.7	-	Vp-p	【Note 7-2】 is over 10kΩ.
	DC component	V_{iDC}	−1.0	0	+1.0	V	[Note 7-3】
Digital input voltage	High level	V_{IH}	+3.7	-	+5.1	V	Input resister is over 10kΩ.
	Low level	V_{IL}	0	-	+1.0	V	[Note 7-4]
	Histeresis	V_H	0.4	-	-	V	
Digital output voltage	High level	V_{OH}	+4.0	-	+5.5	V	Load resister is over 60kΩ.
	Low level	V_{OL}	0	-	+1.0	V	【Note 7-5]
Input horizontal sync. component	freq. NTSC	$f_{H(N)}$	15.13	15.73	16.33	kHz	CLKC="Hi"
	freq. PAL	$f_{H(P)}$	15.03	15.63	16.23	kHz	【Note 7-61
	pulse width NTSC	$\tau_{HI(N)}$	4.2	4.7	5.2	μs	for $\overline{VBS}$ terminal
	pulse width PAL	$\tau_{HI(P)}$	4.2	4.7	5.2	μs	
	rise time	τ_{rHI1}	-	-	0.5	μs	
	fall time	τ_{fHI1}	-	-	0.5	us	
Input vertical sync. component	freq. NTSC	$f_{V(N)}$	$f_H/284$	$f_H/262$	$f_H/258$	Hz	CLKC="Hi", H=1/f_H
	freq. PAL	$f_{V(P)}$	$f_H/344$	$f_H/312$	$f_H/304$	Hz	【Note 7-7 1
	pulse width NTSC	$\tau_{VI(N)}$	-	3H	-	μs	for $\overline{VBS}$ terminal
	pulse width PAL	$\tau_{VI(P)}$	-	2.5H	-	Us	
	rise time	τ_{rVI1}	-	-	0.5	μs	"
	fall time	τ_{fVI1}	-	-	0.5	μs	
Input clock	frequency	f_{CLI}	18.2	18.9	19.6	MHz	SAM="Hi" CLKC="LO"
		f_{CLI}	6.0	6.8	7.6	MHz	SAM=" LO" 【Note 7-81
	'Hi' width	τ_{WH}	20.0	-	-	ns	for CLK terminal
	'Lo' width	τ_{WL}	20.0	-	-	ns	
	rise time	τ_{rCLI}			5.0	Ins	
	fall time	τ_{fCLI}	-	-	5.0	ns	
Input HSY Horizontal sync.)	frequency	f_{HI}	$f_{CLI}/1230$	$f_{CLI}/1200$	$f_{CLI}/1170$	Hz	SAM=" Hi" CLKC="LO"
		f_{HI}	$f_{CLI}/465$	$f_{CLI}/435$	$f_{CLI}/405$	Hz	SAM=" LO" [Note 7-91
	pulse width	τ_{HI}	1.0	4.7	8.4	μs	for $\overline{HSY}$ terminal
	rise time	τ_{rHI1}	-	-	0.05	μs	
	fall time	τ_{fHI1}	-	-	0.05	μs	
Input VSY (Vertical sync.)	frequency	f_V,	50	f_H, /262	f_H I/258	Hz	[Note 7-101 CLKC="LO"
	pulse width	$\tau_{VI(P)}$	1H	3H	5H	μs	for $\overline{VSY}$ terminal
	rise time	τ_{rVI2}	-	-	0.5	μs	
	fall time	τ_{fVI2}	-	-	0.5	μs	
Data set up time		t_{SU1}	25	-	-	ns	[Note 7-111 CLKC="LO"
Dara hold time		t_{HO1}	25	-	-	ns	
Data set up time		t_{SU2}	1.0	I	I	μs	【Note 7-12】
Data hold time		t_{HO2}	1.0	I	I	μs	
DC bias voltage for common electrode driving signal		V_{CDC}	+0. 0	+1.5	+3.0	v	DC component [Note 7-13]
Terminal voltage applicable to brightness		V_{BRT}	+2.0	+2.3	+2.4	V	

[Note 7-11 Power supply voltage should not be changed after adjusting V_{CDC}.

[Note 7-2] VR1, VG1, VB1, VR2, VG2, VB2 terminals (Video signal)

[Note 7-31 VBS, VR1, VG1, VB1, VR2, VG2, VB2 terminals

[Note 7-41 $\overline{HSY}$, $\overline{VSY}$, NTP, VSW, HRV, VRV, SAM CLKC, CLK terminals

[Note 7-51 $\overline{HSY}$, $\overline{VSY}$, CLK terminals (output mode)

[Note 7-61 $\overline{VBS}$ (horizontal sync. component)

[Note 7-7] $\overline{VBS}$ (vertical sync. component)

[Note 7-81 CLK (input mode)

[Note 7-91 $\overline{HSY}$ (input mode)

[Note 7-10] $\overline{VSY}$ (input mode)

[Note 7-111 In case of CLKC=' Hi', it shows the phase difference from $\overline{HSY}$ to CLK. In that case, $\overline{HSY}$ will be taken at the rise timing of CLK.

[Note 7-121 In caseof CLKC=' Hi', it shows the phase difference from $\overline{VSY}$ to $\overline{HSY}$. In that case, $\overline{VSY}$ will be taken at the rise timing of $\overline{HSY}$.

[Note 7-131 Adjusting the optimal voltage every module at the typical value of power supply voltage to get the maximum value of contrast. However, in the case that the power supply voltage is changed, for example, the level of power supply voltage is reduced, please adjust it externally to get the best contrast with a resistor you add to this terminal, or semifixed resistor, VCDC, in module. A recommended circuit is shown in Fig. 5.

7-2) Power consumption

Table 6 T a= 25°C

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Remarks
Positive supply current	I_{SH}	$V_{SH}=+8.0V$	-	120	160	mA	
Negative supply current	I_{SL}	$V_{SL}=-5.0V$	-	40	55	mA	
Total	W_S			**1.2**	1.6	w	

7-3) Circuit diagram

The circuit block diagram of TFT-LCD module is shown in Fig. 4.

BRT, V_{CDC}, external adjusting recommended circuit is shown in Fig. 5.

Caution: Turn on or off the power supply (V_{SH} and V_{SL}) at the same time. Be careful to supply all power voltage before inputting signals.

7-4) Input/output signal waveforms.

They are shown in Fig. 6-A, B, C.

Caution: For theVBS signal, input standard composite video (or sync.) signal applicable to the operating mode which have NTSC(M) or PAL(B·G) and is selected by the NTP signal.

A long time input of non-standard sync. signal may cause flicker or degradation of display quality.

7-5) Input/Output signal timing chart

It is shown in fig. 6-A, B

Table 7 (CLKC="Hi"、NTSC:f_H=15.7kHz、f_V=60Hz／PAL:f_H=15.6kHz、f_V=50Hz)

Parameter		Symbol	MIN	TYP	MAX	Unit	Remarks
Horizontal sync. output pulse	pulse width	τ_{HS2}	2.9	3.9	4.9	μs	f=f_H [Note 7-201
	phase difference	r pd	0.1	1.1	2.1	μs	[Note 7-21]
	rise time	τ_{rHO}	–	–	0.5	μs	C_L=10pF
	fall time	τ_{fHO}	–	–	0.5	μs	
Vertical sync. output pulse	pulse width	τ_{VS}	-	4H	-	μs	1H=1/f_H
	phase difference	τ_{VHO}	-	11.0	28.0	μs	[Note 7-221
	rise time	τ_{rVO}	-		2.0	μs	CL=1OPF
	fall time	τ_{fVO}	-		2.0	μs	
‘Vertical phase difference	odd field	τ_{PV1}	-	1 H	-	μs	1H=1/f_H
	even field	τ_{PV2}	–	0.5H	-	μs	[Note 7-231

(Supply voltage condition:V_{SH}=+8. 0V, V_{SL}=-5. 0V)

[Note 7-201 Adjusted by variable resister (H-POS) in a module.

[Note 7-211 Variable range by variable resister (H-POS) in a module.

adjustment : $\tau pd = 1.1 \pm 0.7$ μs

[Note 7-221 Synchronized with $\overline{HSY}$, based on falling timing of $\overline{HSY}$.

[Note 7-23] $\overline{VSY}$ signal delays.

7-6) Display time range

① NTSC(M) mode (NTP='Hi', CLKC=' Hi')

Displaying the following range within video signals.

(a) Horizontally : 12.2 ~ 63.0 μs from the falling edge of HSY.(SAM='Hi')

: 12.3- 62.9 μs from the falling edge of HSY. (SAM=' Lo')

(b) Vertically : 20 ~ 253 H from the falling edge of VSY.

② PAL(B·G) mode (NTP=' Lo', CLKC='Hi')

Displaying the following range within video signals.

(a) Horizontally : 13.0 ~ 63.8 μs from the falling edge of $\overline{\text{HSY}}$.(SAM=' Hi')

13.1 ~ 63.7 μs from the falling edge of $\overline{\text{HSY}}$.(SAM=' Lo')

(b) Vertically : 2 6 - 298 H from the falling edge of $\overline{\text{VSY}}$.

However, the video signals of (14n+12)H, (14n+20)H/Even field.

(14n+17)H, (14n+23)H/Odd field (n=1, 2··●, 20)

are not displayed on the module.

③ External clock mode (NTP='Hi', CLKC=' Lo')

Displaying the following range within video signals.

(a) Horizontally : 205 ~ 1164 clk from the falling edge of $\overline{\text{HSY}}$.(SAM=' Hi')

: 84 ~ 403 clk from the falling edge of $\overline{\text{HSY}}$.(SAM='Lo')

(elk means input external clock.)

(b) Vertically : 20 ~ 253 H from the falling edge of $\overline{\text{VSY}}$.

(8)Optical characteristics

Table? Ta=25℃

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remarks.
Viewing angel range		Δθ11	CR≧10	30	-	-	“ (degree)	
		Δθ12		10	-	-	“ (degree)	
		Δθ 2		45	-	-	“ (degree)	[Note 8-1,21
Contrast ratio		CRmax	Optimal	60	-	-		[Note 8-2, 3]
Response time	Rise	rr	θ=0°	-	30	60	ms	[Note 8-2,4]
	Fall	rd			50	100	ms	
Transsmision		Tr	θ=0°	4.1	4.8	-	%	[Note 8-5]
Chromaticity shift		Ax		-0.025	-	+0.045		[Note 8-6]
		Δy		-o. 010		+0.05C		
Reflection		Rf	θ=12°	-	1.5	3.5	%	

[Note 8-n Viewing angle range is defined as follows.

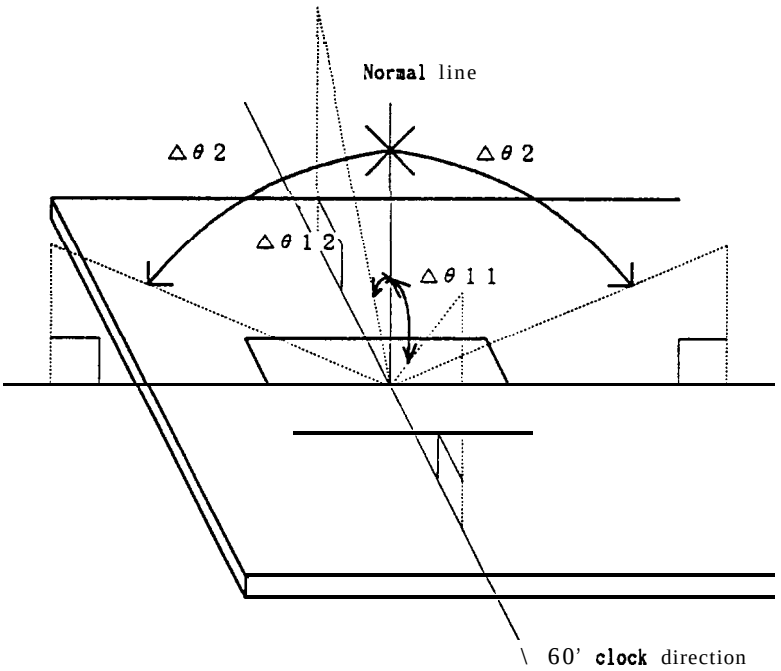


Fig.(i) Definition of viewing angle

【Note 8-2】 Applied voltage condition:

i) V_{CDC} is adjusted so as to attain maximum contrast ratio.

ii) Terminal adjustable to brightness (BRT) is open.

iii) Input video signal of standard black level and 100% white level.

[Note 8-31 Contrast ratio is defined as follows:

$$\text{Contrast ratio(CR)} = \frac{\text{Photodetector output with LCD being "white"}}{\text{Photodetector output with LCD being "black"}}$$

【Note 8-41 Response time is obtained by measuring the transition time of photodetector output, when input signals are applied so as to make the area "black" to and from "white".

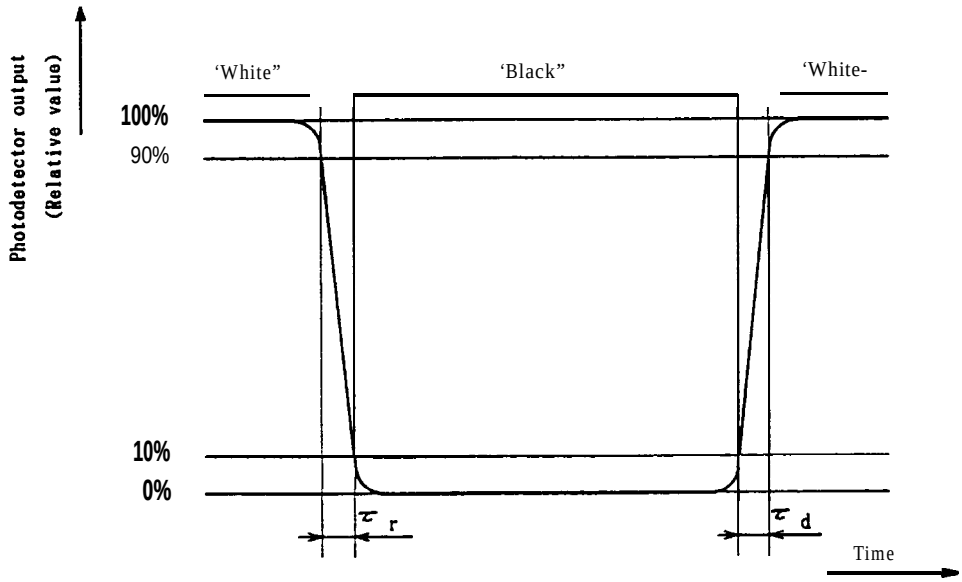


Fig. (ii)

[Note 8-5] Transmission is defined as follows.

$$\text{Transmission} = \frac{\text{Photodetector out put voltage when measuring the brightness of theLCD panel placed on the light source with not applied voltage}}{\text{Photodetector output voltage when measuring the light source brightness}}$$

[Note 8-61 Chromaticity shift is the difference of that of the light source and the panel placed on it.

(In the case that the light source chromaticity(x=0. 310, Y=O. 316)

(9)Mechanical characteristics

9-1) External appearance

Do not exist extreme defects. (See Fig. 3)

9-2) Panel toughness

The panel shall not break, when 19N is pressed on the center of the panel by a smooth sphere having 15 mm diameter.

Caution: In spite of very soft toughness, be careful if, in the long-term, add pressure on the active area and as it is possible for the functional damage to occur.

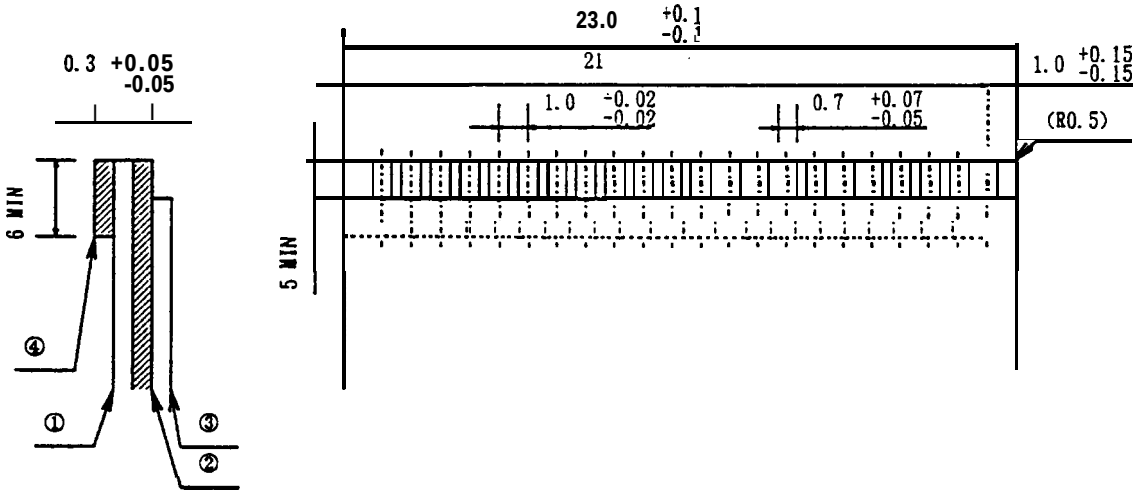
9-3) Input/output connector performance

A)Input/output connectors for the operation of LCD module (FPC connector 22 pin) inapplicable FPC Shown in Fig.(i).

ⅰ)Terminal holding force More than 0.9N/pin

(Each terminal is pulled out at a rate of 25 ±3mm/min.)

ⅱ)Insertion/pulling:contact resistance is not twice larger than the durability initial value after applicable FPC is inserted and pulled out 20 times



No.	N a m e	Materials
①	Base material	Polyimide or equivalent material(25μm thick)
②	Copper foil	Copper foil(35μm thick) Solder plated in 2 to 12μm
③	Cover lay	Polyimide or equivalent material
④	Reinforcing plate	Polyester polyimide or equivalent material(188μm thick)

Fig. (ⅰ)FPC applied to input/output connector (1.0mm pitch)

(10) Display quality

The display quality of the color TFT-LCD module shall be in compliance with the Delivery Inspection Standard.

(11) Handling instructions

11-1) Mounting of module

The TFT-LCD module is designed to be mounted on equipment using the mounting tabs in the four corners of the module at the rear side.

On mounting the module, as the M2.6 tapping screw (fastening torque is 0.3 through 0.5N·m) is recommended, be sure to fix the module on the same plane, taking care not to wrap or twist the module. Please power off the module when you connect the input/output connector.

11-2) Precautions in mounting

① Polarizer which is made of soft material and susceptible to flaw must be handled carefully. Protective film (Laminator) is applied on the surface to protect it against scratches and dirts. It is recommended to peel off the laminator immediately before the use, taking care of static electricity.

② Precautions in peeling off the laminator

A) Working environment

When the laminator is peeled off, static electricity may cause dust to stick to the polarizer surface. To avoid this, the following working environment is desirable.

a) Floor:Conductive treatment of 1MΩ or more on the tile
(conductive mat or conductive paint on the tile)

b) Clean room free form dust and with an adhensive mat on the doorway

c) Advisable humidity:50%～70% Advisable temperature:15℃～27℃

d) Workers shall wear conductive shoes, conductive work clothes, conductive gloves and an earth band.

B) Working procedures

a) Direct the wind of discharging blower somewhat downward to ensure that module is blown sufficiently. Keep the distance between module and discharging blower within 20 cm. (See Fig. (k-i).)

b) Attach adhensive tape to the laminator part near discharging blower so as to protect polarizer against flaw. (See Fig. (iv-ii).)

c) Peel off laminator, pulling adhensive tape slowly to your side taking 5 or more second.

d) On peeling off the laminator, pass the module to the next work process to prevent the module to get dust.

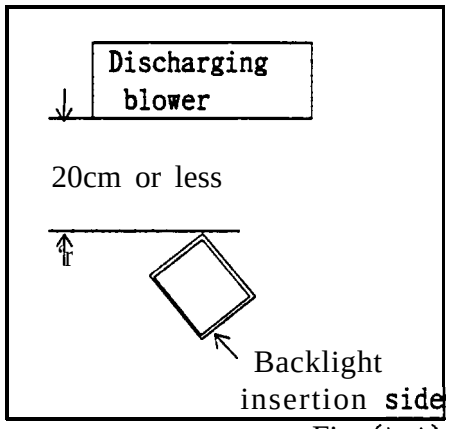


Fig. (iv-i)

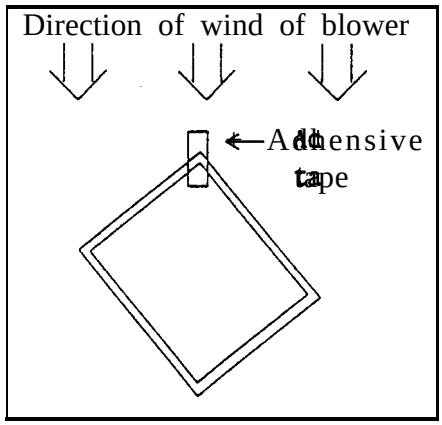


Fig. (i-i)

Fig. (iv)

e) Method of removing dust from polarizer

.Blow off dust with N_2 blower for which static electricity preventive measure has been taken. Ionized air gun (Hugle Electronics Co.) is recommended.

·Since polarizer is vulnerable, wiping should be avoided.
But when the panel has stain or grease, we recommend to use adhesive tape to softly remove them from the panel.

③ When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth. For stubborn dirts, wipe the part, breathingon it.

④ Wipe off water drop or finger grease immediately. Long contact with water may cause discoloration or spots.

⑤ TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Handle with care.

⑥ Since CMOS LSI is used in this module, take care of static electricity and earth your body when handling.

11-3) Precautions in. adjusting module

Adjusting volumes on the rear face of the module have been set optimally before shipment. Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described here may not be satisfied.

11-4) Guide line of the backlight design

① Luminance on panel surface:5000 cd/m² or less.
Wave length to cut less than 400nm wave length.

② Panel surface temperature should not exceed 85℃ from the lamp heat.

③ Please refer to the appendix 3 for mechanical design of reflection plate.

④ TFT module dose not have countermeasure of the radiation noise from the lamp. Please prevent them by the backlight side.

* Diffuser is incorporated with module.

11-5) Caution of product design

① The LCD module shall be protected against water salt-water by the waterproof cover.

② Please take measures to interferential radiation from module, to do not interfere surrounding appliances.

11-6) Others

① Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours; liquid crystal is deteriorated by ultraviolet rays.

② Store the module at a temperature near the room temperature. At lower than the rated storage temperature, liquid crystal solidifies, causing the panel to be damaged. At higher than the rated storage temperature, liquid crystal turns into isotropic liquid and may not recover.

③ If LCD panel breaks, there maybe a possibility that the liquid crystal escapes from the panel. Since the liquid crystal is injurious, do not put it into the eyes or mouth. When liquid crystal sticks to hands, feet or clothes, wash it out immediately with soap.

④ Observe all other precautionary requirements in handling general electronic components.

(12) Shipping requirements

12-1) Packing form is shown in Fig. 8.

12-2) Carton storage condition

① Number of layers of cartons in pile : 10 layers max.

② Environmental condition :

"Temperature	0 ℃ to 40 ℃
"Humidity	60 %RH or less (at 40 ℃) No dew condition even at a low temperature and high humidity
"Atmosphere	Harmful gases such as acid and alkali which corrode electronic components and wires must not be detected.
"Storage period	About 3 months
"Opening of package	To prevent TFT-LCD module from being damaged by static electricity, adjust the room humidity to 50 %RH or higher and provide an appropriate measure for electrostatic earthing before opening the package.

(13) Reliability test items

Reliability test items for the TFT-LCD module are shown in Table 9.

(14) Others

14-1) Indication of lot number

Attached location of label : See Fig. 3.

Indicated contents of the label

LQ5RA43 OOOOOOOO

Model number Lot number

1 place : Produced year (ex. 1995 ⇨ 5)

2 place : Produced month (1, 2, 3, ……, 9, X, Y, Z)

3~7 place : Serial number (00001-)

8 place : Revisional sign (A, B, C, ……)

Reliability test Items for TFT-LCD Module

Table 9

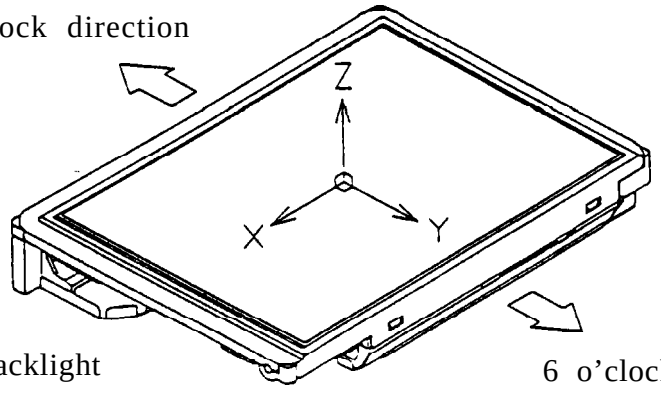
No	Test items	Test conditions
1	High temperature storage test	Tp= + 85℃ 240h
2	Low temperature storage test	TP= – 30℃ 240h
3	High temperature and high humidity operating test	Tp= + 60℃.90~95%RH 240h
4	High temperature operating test	Tp= + 85℃ 240h
5	Low temperature operating test	Tp= – 30℃ 240h
6	Electrostatic discharge test	±200V·200pF(0Ω), Once for each terminal.
7	Shock test	980m/s²·6ms, ±X, ±Y, ±Z 3 times for each direction (JIS C0041, A-7 Condition C)
8	Vibration test	Frequency range: 8-33. 3Hz Stroke 1. 3mm. Sweep · 33. 3Hz~400Hz Acceleration : 28. 4m/s² Frequency : 15min 2 hours for each direction of X, Z [Note 13-11 4 hours for direction of Y (8 hours in total) (JIS D1601)
9	Heat shock test	−30℃～+85℃／200cycles (0. 5h) (O. 5h)

【Note】 Tp=Panel temperature

【Result Evaluation Criteria]

Under the display quality test conditions with nomal operation state, there shall be no change which may affect practical display function.

[Note 13-1] Direction of X. Y, Z is defined as follows.



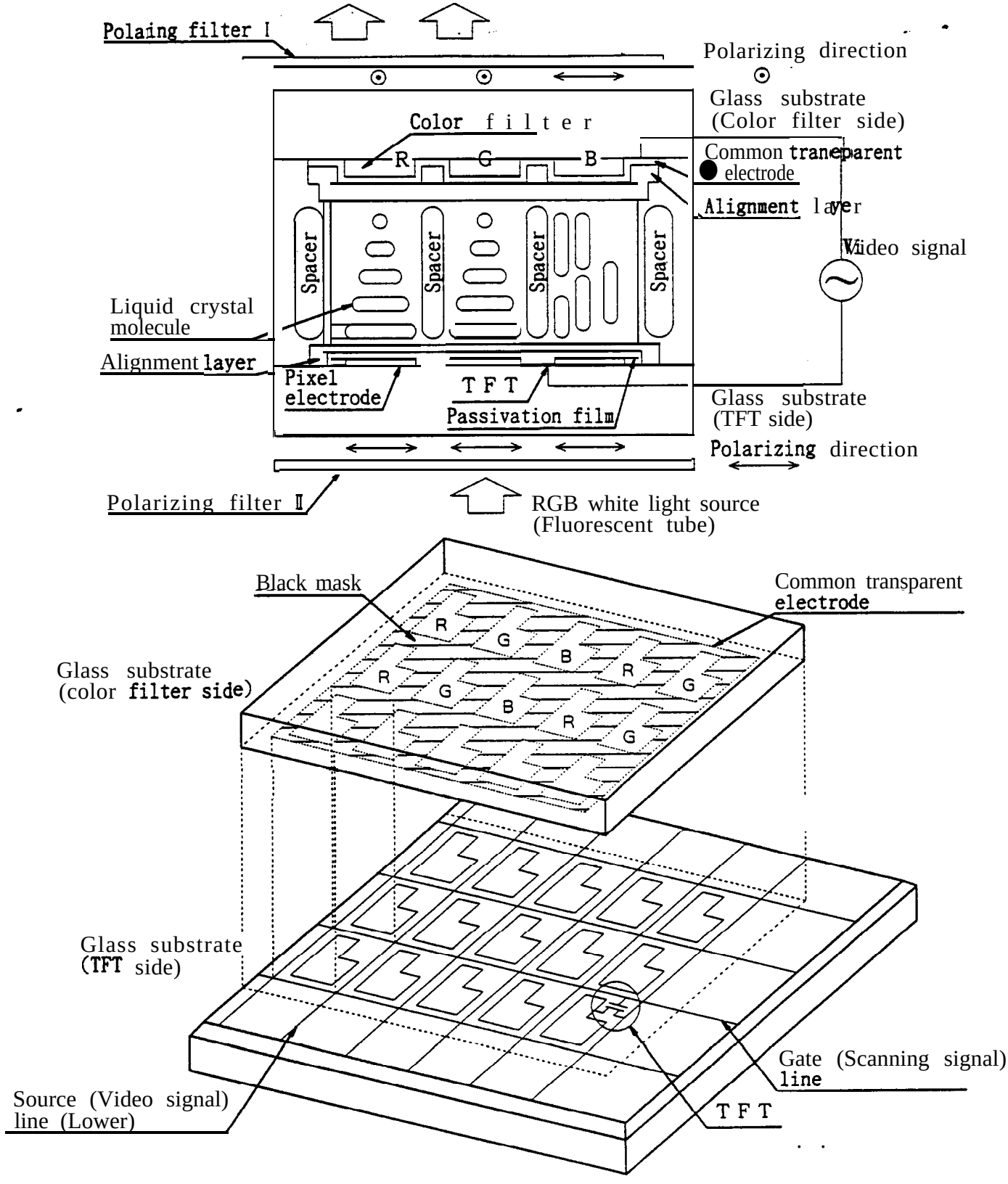


Fig. 1. Illustration of TFT-LCD panel

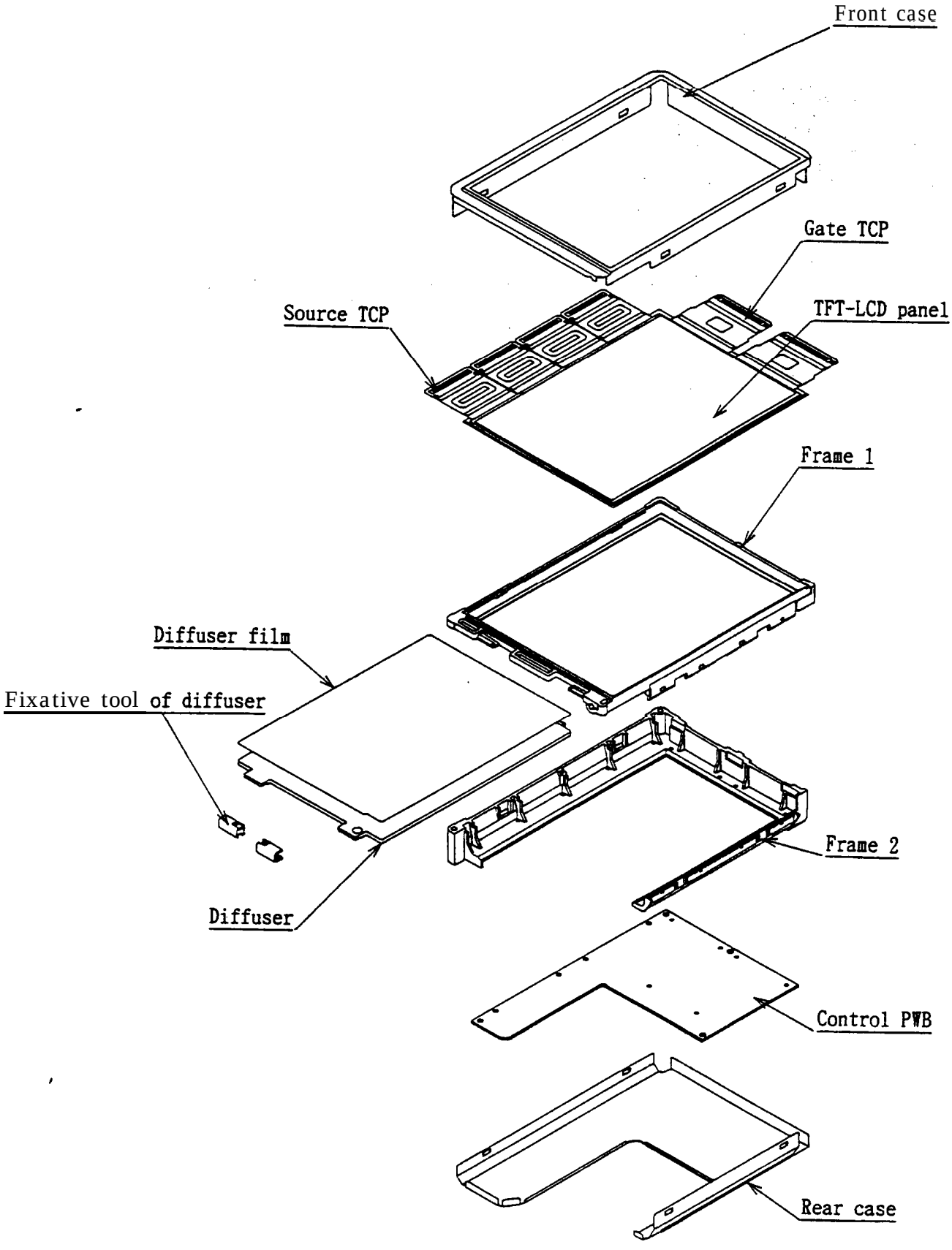


Fig. 2. Construction of TFT-LCD module

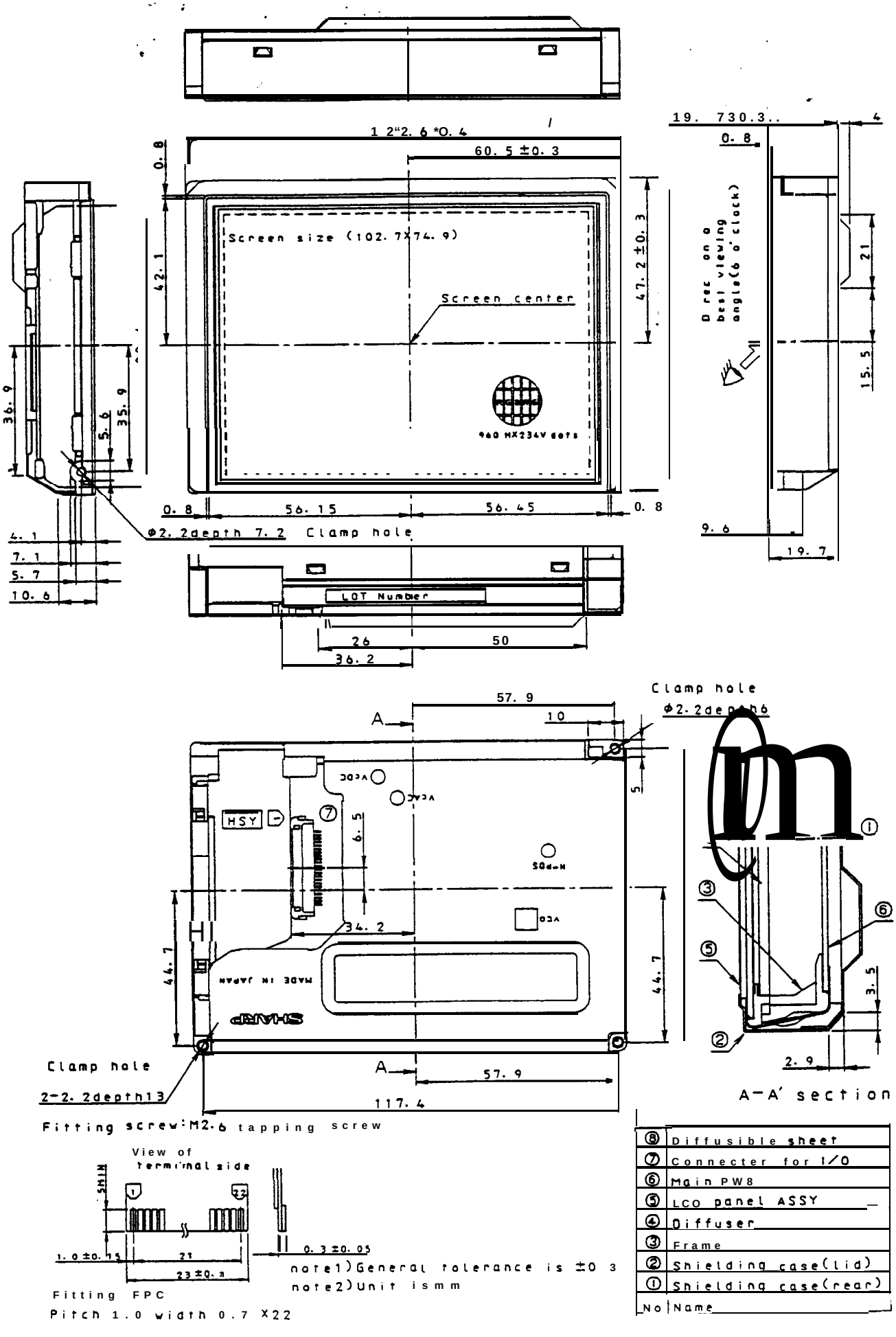


Fig. 3. Outline dimensions of TFT-LCD moudule

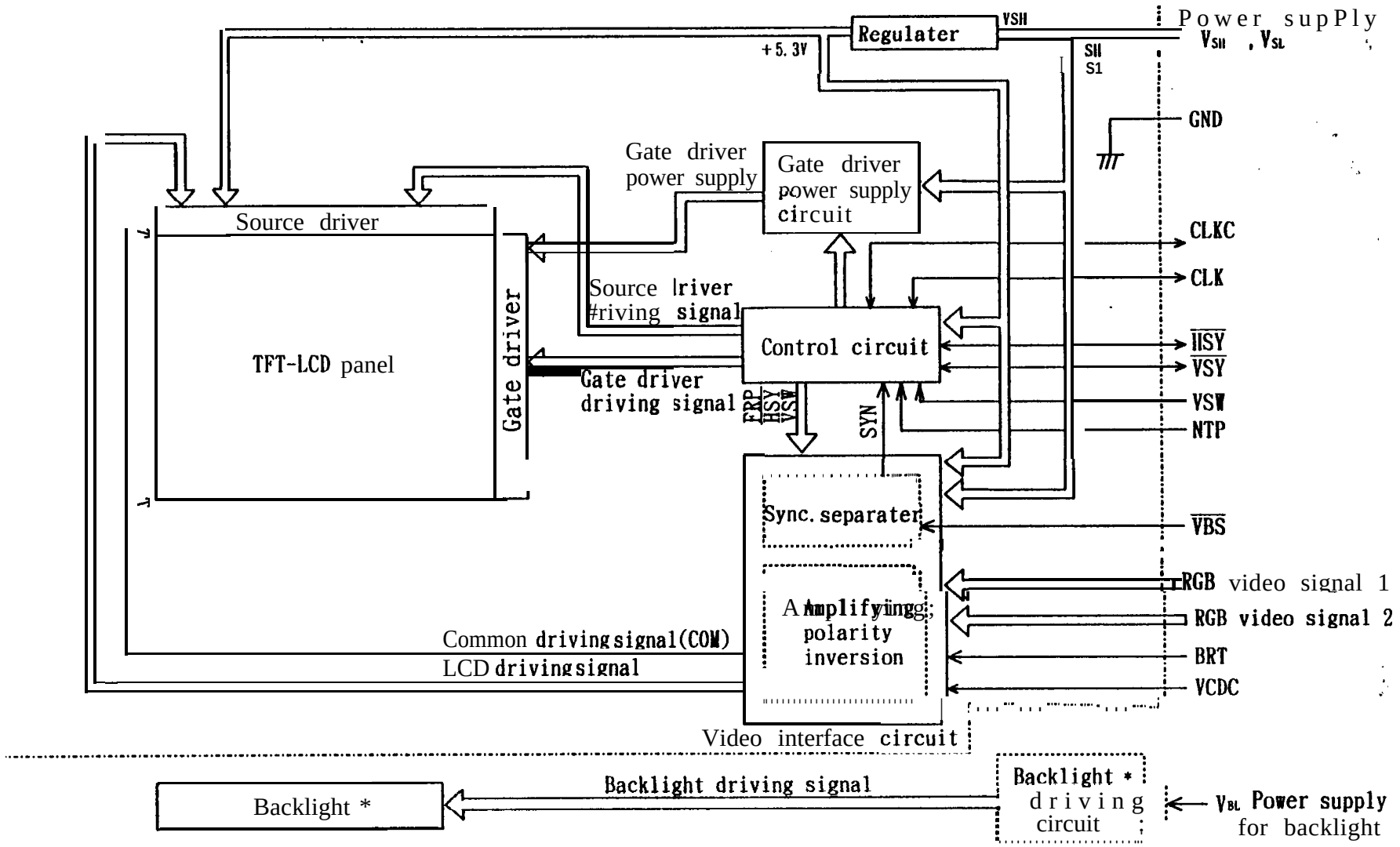


Fig. 4. Circuit block diagram of TFT-LCD module

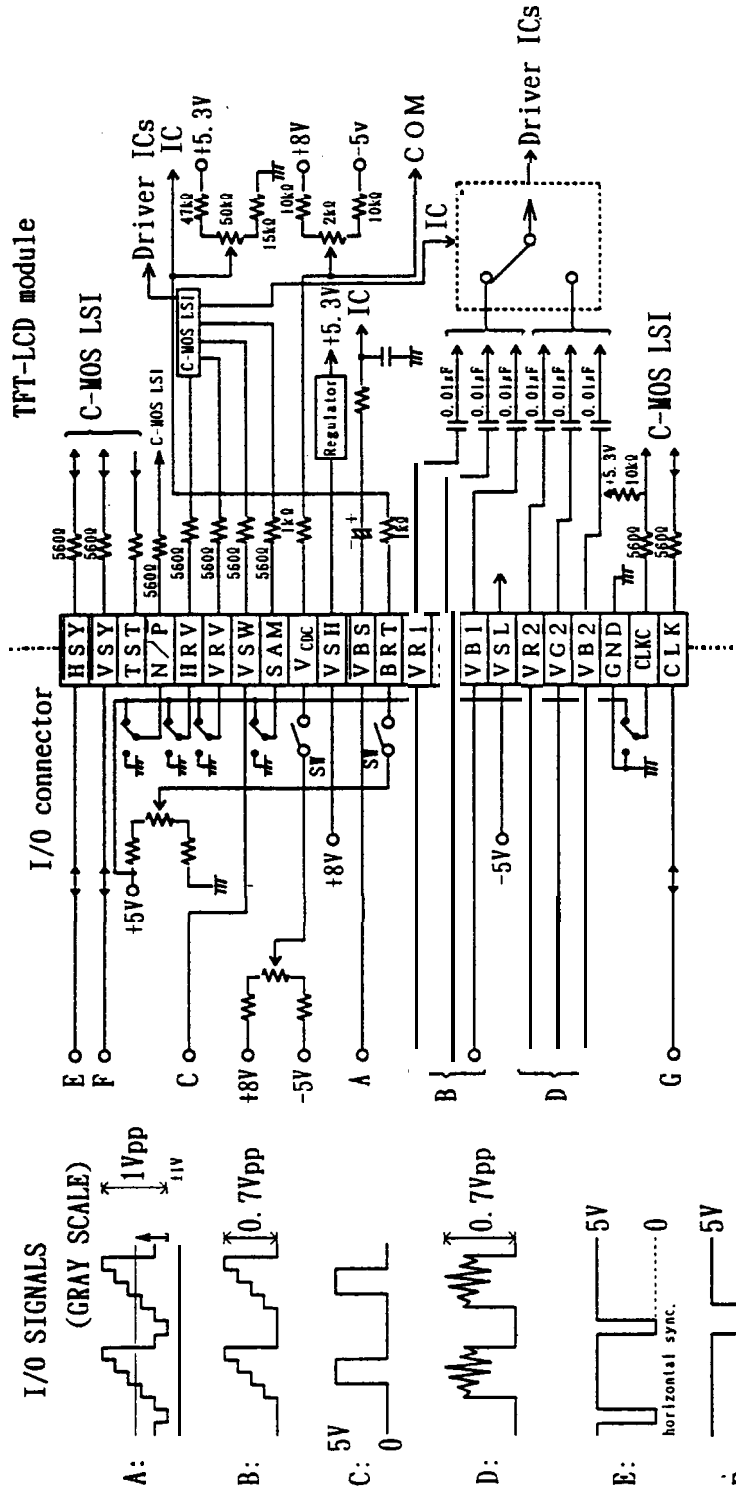


Fig. 5 Recommended circuit to refer

(Note)
input impedance of A, B, D: >10kΩ
input impedance of C: >50kΩ

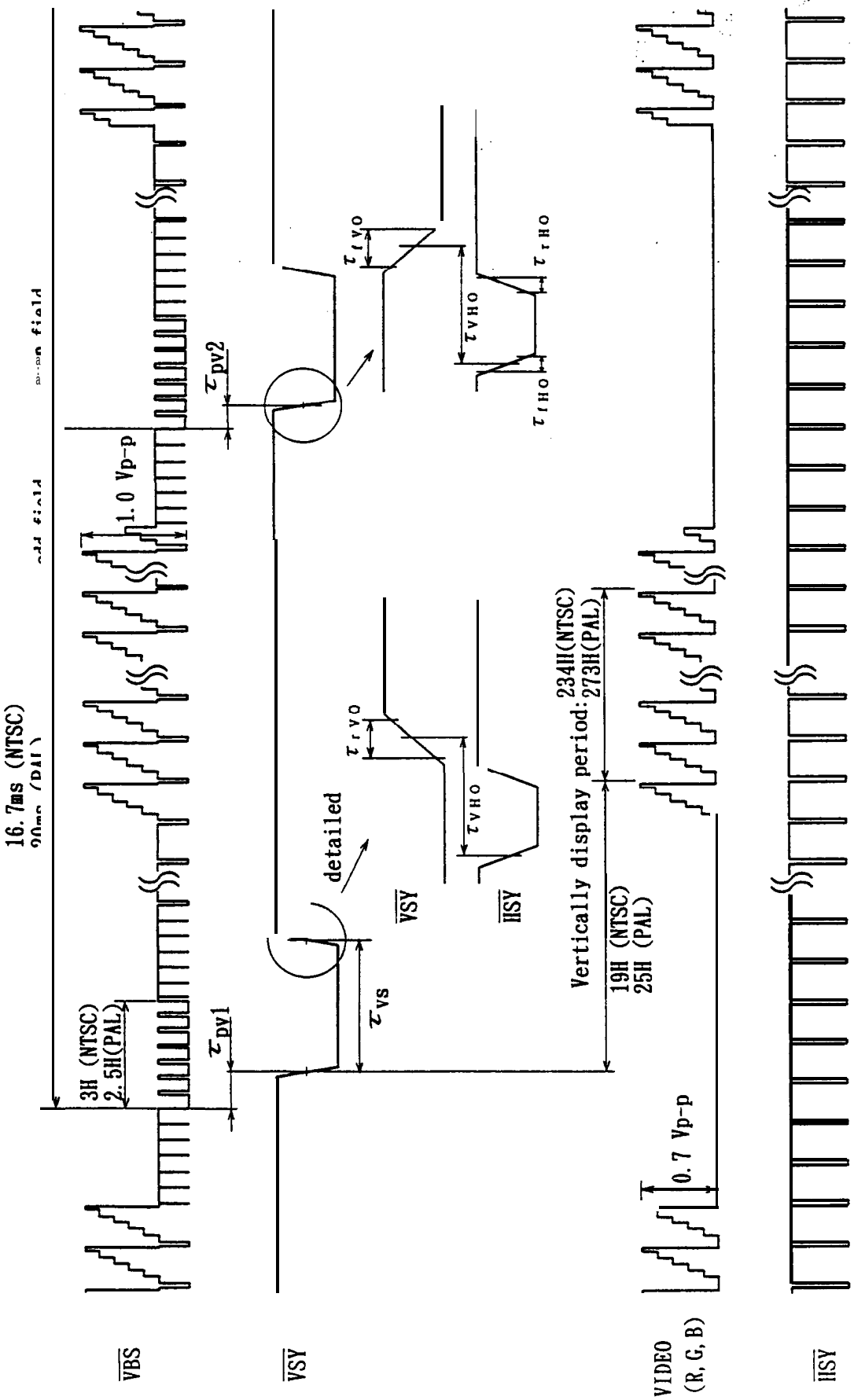


Fig. 6-A. Input/Output signal waveforms (CLKC="Hi")

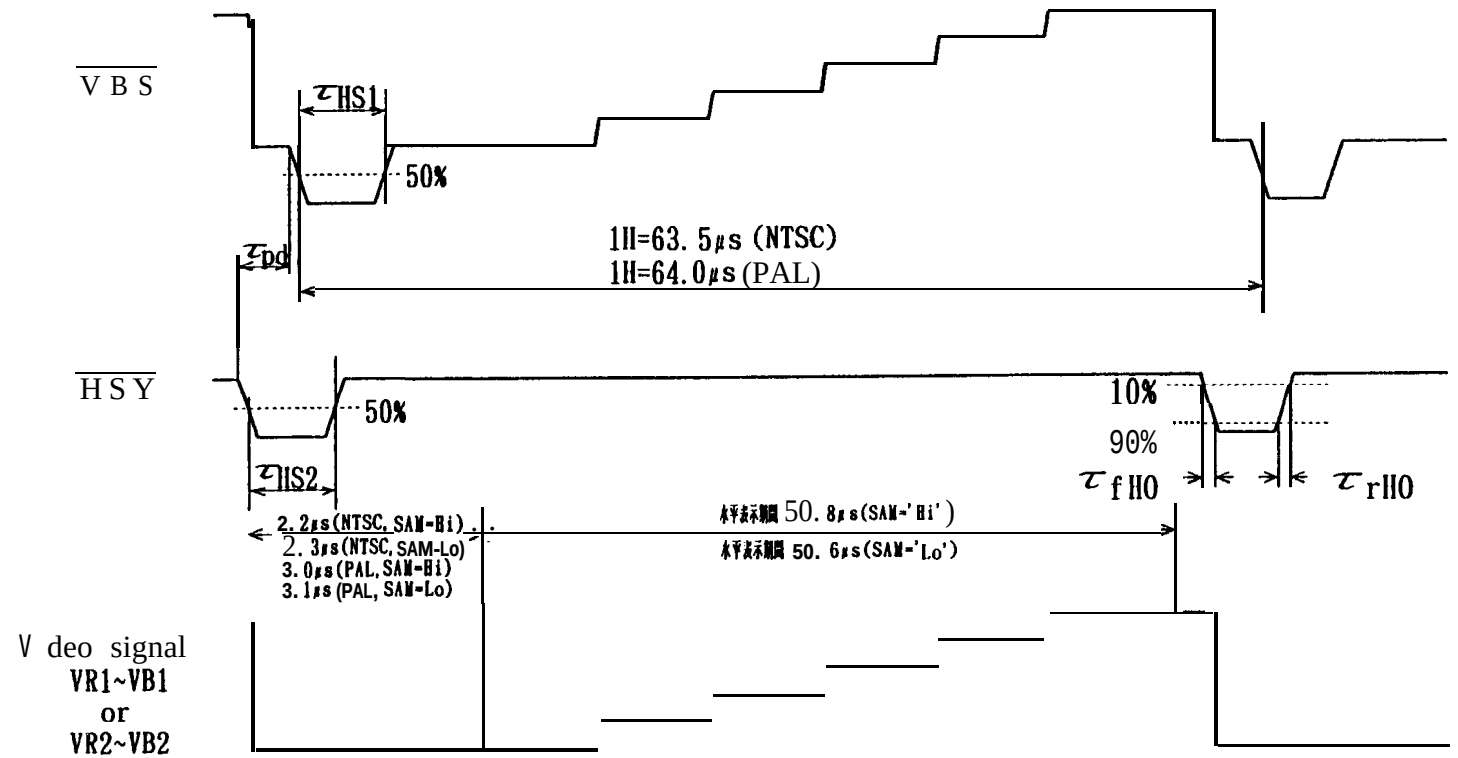


Fig. 6-B. Input/Output signal waveforms (CLKC="Hi")

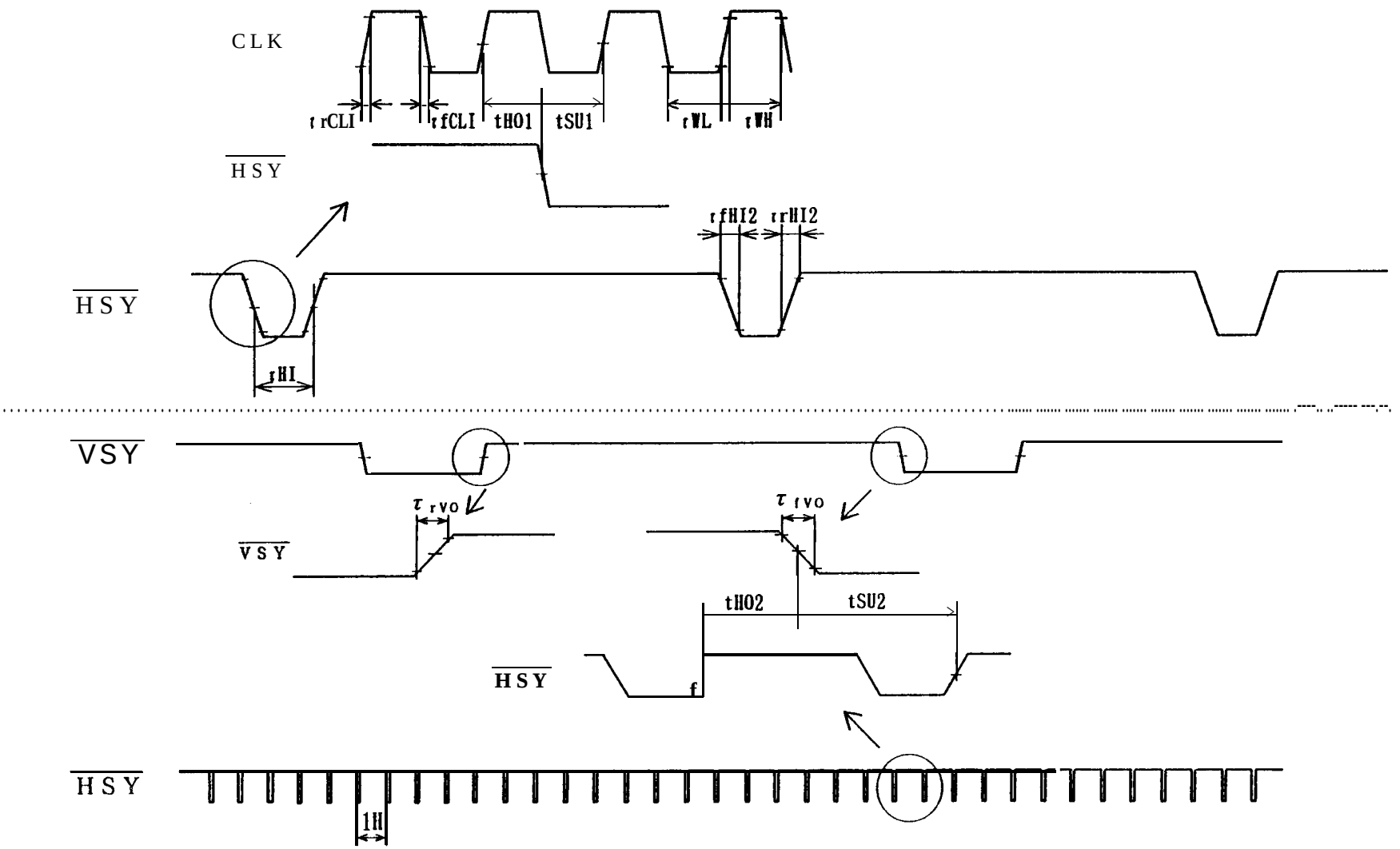
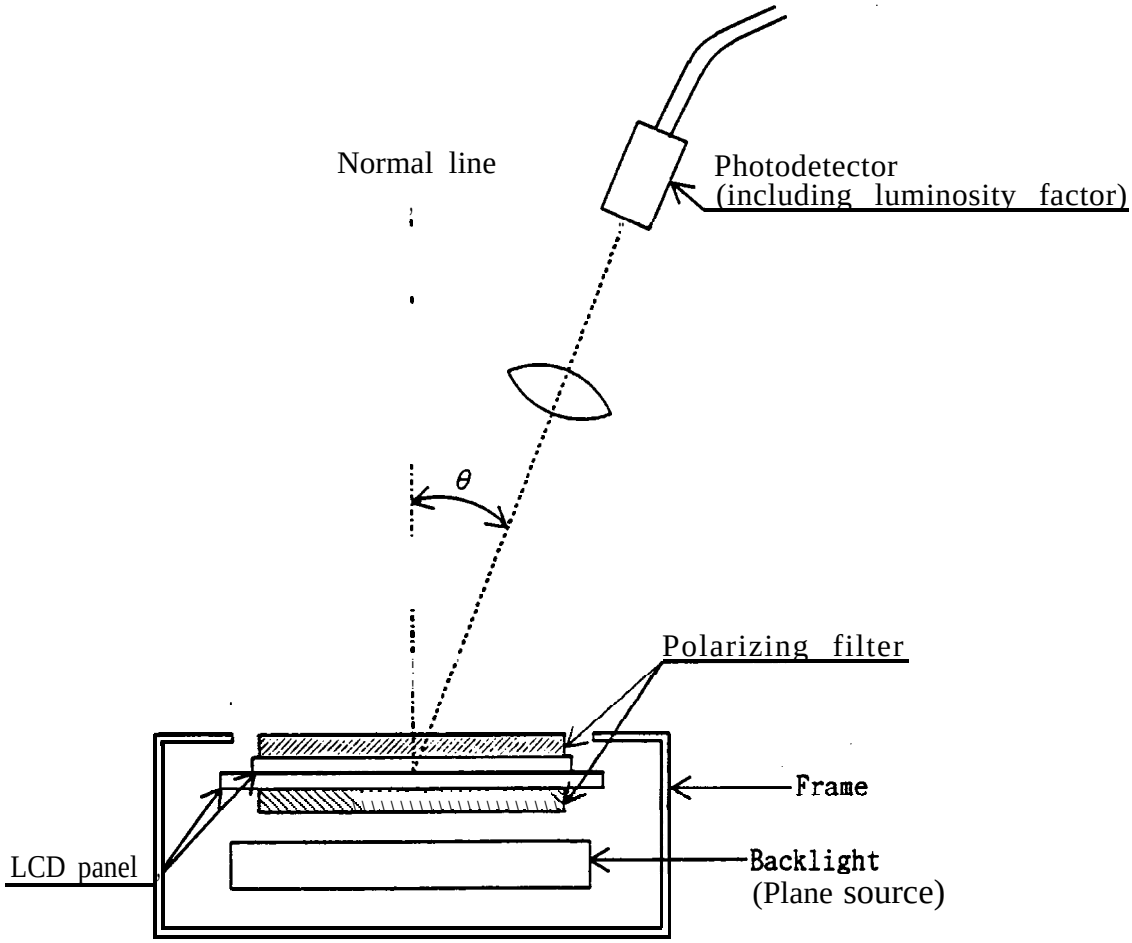


Fig. 6-C. Input/Output signal **waveforms (external clock mode NTP="Hi" CLKC="** Lo")



Brightness : Less than 5000cd/m²
Wave length: To cut less than 400nm

Fig. 7. Optical characteristics

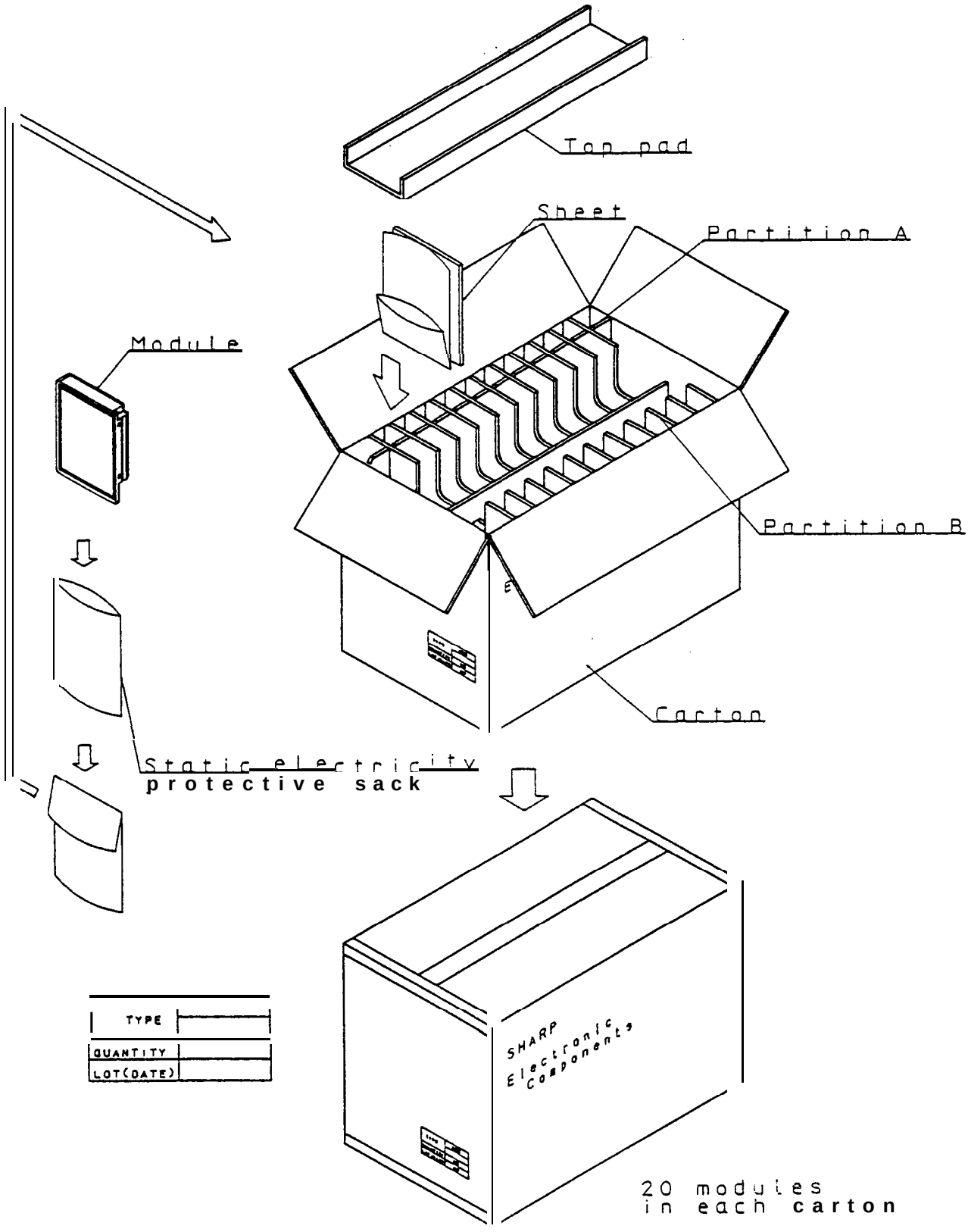


Fig. 8. Packing form

(Appendix-l)" Adjusting method of optimum common electrode DC bias voltage

To obtain" optimum DC bias voltage of common electrode driving signal(V_{CDC}), photo-electric devices are very effective, and the accuracy is within O. 1V. . . .

(In visual examination method, the accuracy is about 0.5V because of the difference among individuals.)

To gain optimum common electrode DC bias voltage, there is the following method which use photo-electric device.

(Measurement of flicker}

DC bias voltage is adjusted so as to minimize NTSC:60HZ(30HZ) PAL:50Hz(25Hz) flicker.

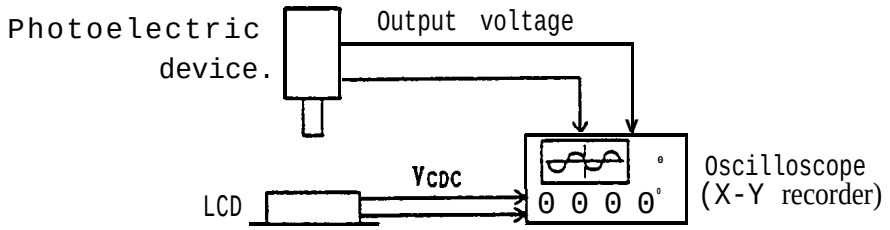
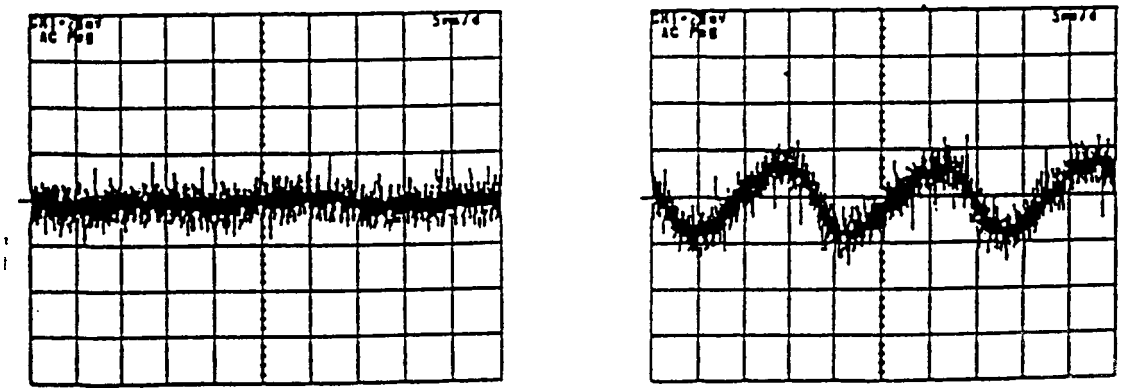


Fig. A Measurement system

Photo-electric output voltage is measured by an oscilloscope at a system shown in Fig. A. DC bias voltage must be adjusted so as to minimize the NTSC: 60Hz(30Hz) PAL: 50Hz(25Hz) flicker with DC bias voltage changing slowly. (Fig, B)



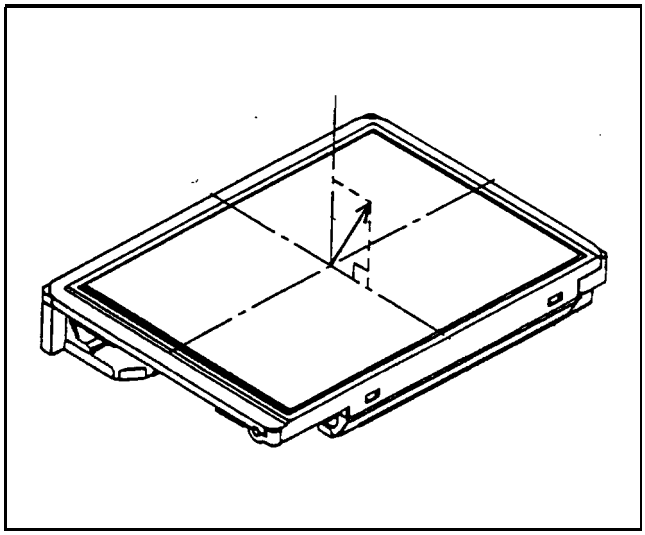
DC bias : Optimum

DC bias: Optimum+ 1V

Fig. B Waveforms of flicker

(Appendix-2) Electrical display rotating function

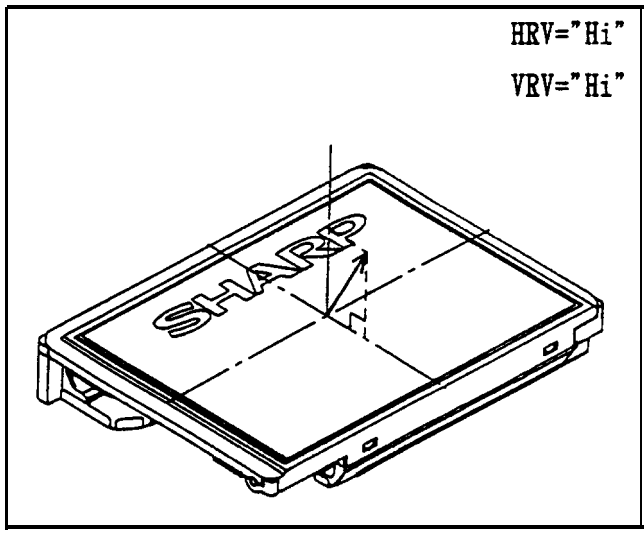
This module LQ5RA43 has a following optical characteristics.
And the optimum viewing angle is 6 o'clock direction.



- Direction of arrow : optimum viewing angle

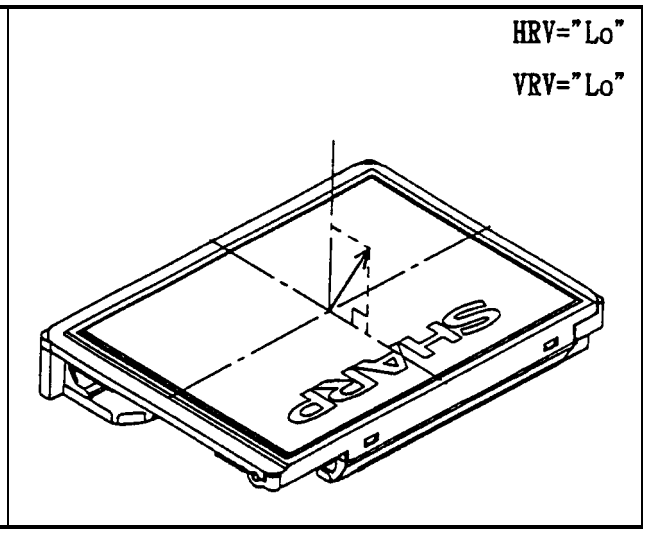
Fig. C. 6 o'clock viewing angle panel

Basically this TFT-LCD module LQ5RA43 has the 6 o'clock viewing angle panel as above. However, it is also possible to use as 12 o'clock viewing angle type by using "Electrical display rotating function" **as** follows; (at this moment, it is necessary to rotate the module 180° mechanically.)



Direction of arrow : optimum viewing angle

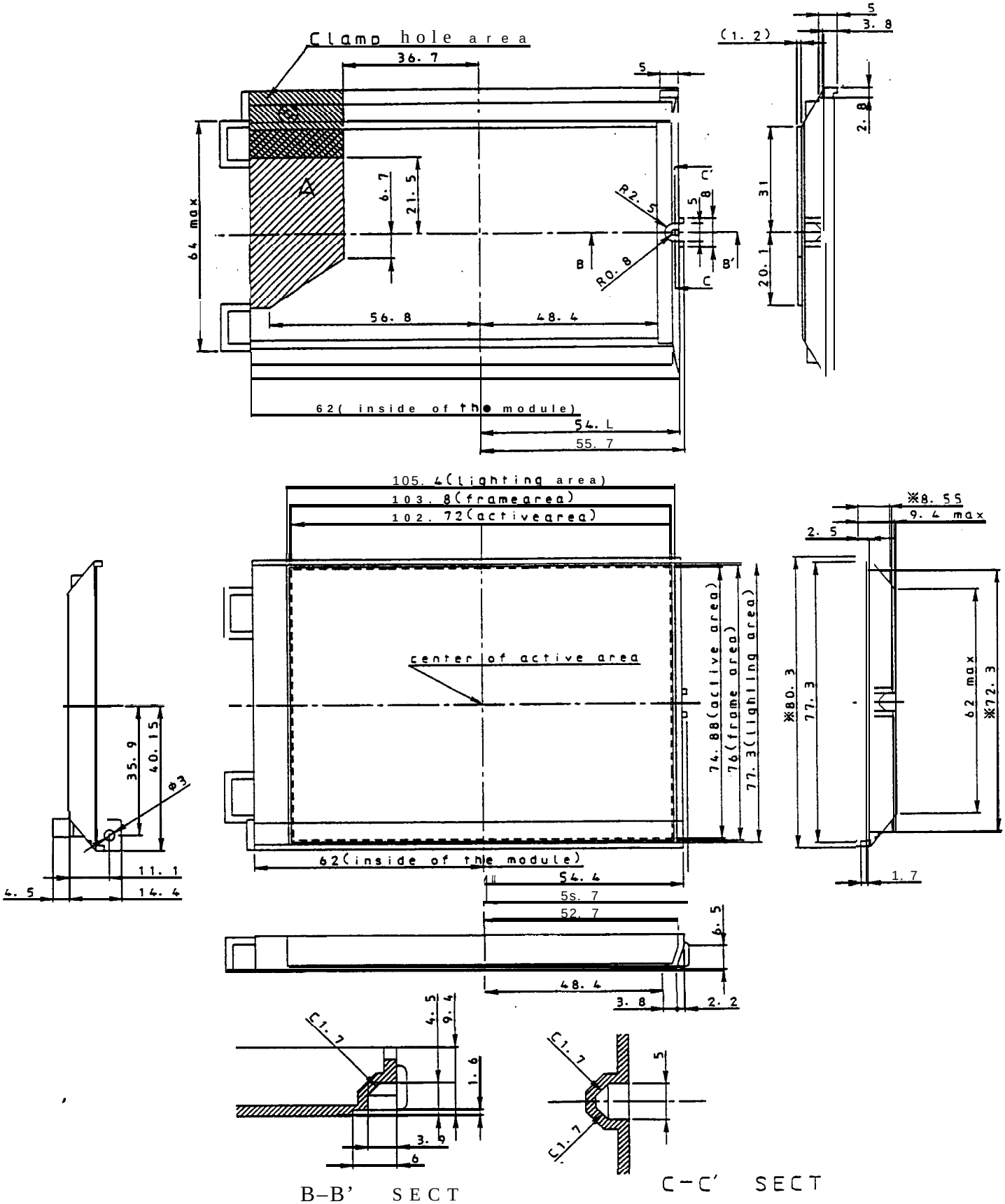
Fig. D. 6 o'clock direction type



Direction of arrow : optimum viewing angle

Fig. E. 12 o'clock direction type -

(Appendix-3) Reference plan of Backlight reflector



B–B' SECT

C–C' SECT

1) 1.2mm of the height (thickness) of shadow area A is the referred one till the surface of PWB.
2) ※ is the connecting length with frame.
3) Please shield the noise out of lamp, or it' 11 badly effect the image.